WE CLAIM:

1. An integrated circuit, comprising:

a semiconductor substrate having a first area and a second area, where the second area is adjacent to the first area;

a first transistor gate electrode formed over the substrate in the first area;

a second transistor gate electrode formed over the substrate in the second area;

a first gate dielectric layer disposed between the first transistor gate electrode and the substrate, where the first gate dielectric layer includes a layer of silicon nitride that is sufficiently thin to permit the oxidation of underlying silicon therethrough; and

a second gate dielectric layer disposed between the second transistor gate electrode and the substrate, the second gate dielectric layer having a thickness that is different than the equivalent thickness of the first gate dielectric layer.

2. The integrated circuit of Claim 1, wherein the second gate dielectric layer comprises silicon oxide.

3. The integrated circuit of Claim 1, wherein the second gate dielectric layer has a thickness that is greater than the equivalent thickness of the first gate dielectric layer.

4. The integrated circuit of Claim 1, wherein the first gate dielectric layer further comprises a silicon oxide layer disposed between the silicon nitride layer and the substrate in the first area.

5. The integrated circuit of Claim 4, wherein the first gate dielectric layer further comprises an oxide layer disposed over the silicon nitride layer.

6. The integrated circuit of Claim 1, wherein a plurality of memory arrays are formed in the second area of the substrate.

7. The integrated circuit of Claim 6, wherein a logic control circuit is formed in the first area of the substrate.

8. The integrated circuit of Claim 7, wherein the first area is formed at the periphery of the second area.